

BSS138

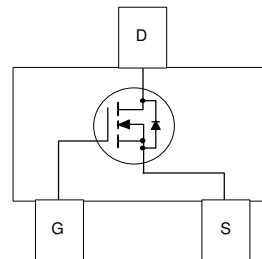
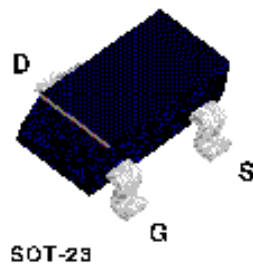
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- 0.22 A, 50V. $R_{DS(ON)} = 3.5\Omega @ V_{GS} = 10V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- Rugged and Reliable
- Compact industry standard SOT-23 surface mount package.



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	BSS138	Units
V_{DS}	Drain-Source Voltage	50	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 20K\Omega$)	50	V
V_{GSS}	Gate-Source Voltage - Continuous	± 20	V
	- Non Repetitive ($T_p < 50 \mu\text{S}$)	± 40	
I_D	Drain Current - Continuous	0.22	A
	- Pulsed	0.88	
P_D	Maximum Power Dissipation	0.36	W
	Derate Above 25°C	2.8	mW/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	350	$^\circ\text{C}/\text{W}$
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Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	50			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 50 V, V _{GS} = 0 V			0.5	μA
		T _J =125°C			5	μA
		V _{DS} = 30 V, V _{GS} = 0 V			100	nA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 1 mA	0.8	1.3	1.6	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.22 A		0.81	3.5	Ω
		V _{GS} = 4.5 V, I _D = 0.22 A		1.16	6	
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 0.22 A	0.12	0.45		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		30	60	pF
C _{oss}	Output Capacitance			15	25	pF
C _{rss}	Reverse Transfer Capacitance			7.5	10	pF
SWITCHING CHARACTERISTICS (Note 1)						
t _{D(on)}	Turn - On Delay Time	V _{DD} = 30 V, I _D = 0.29 A, V _{GS} = 10 V, R _{GEN} = 50 Ω			8	ns
t _r	Turn - On Rise Time				12	ns
t _{D(off)}	Turn - Off Delay Time				16	ns
t _f	Turn - Off Fall Time				22	ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Source Current				0.22	A
I _{SM}	Maximum Pulse Source Current (Note 1)				0.88	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.44 A		0.8	1.4	V

Note:

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

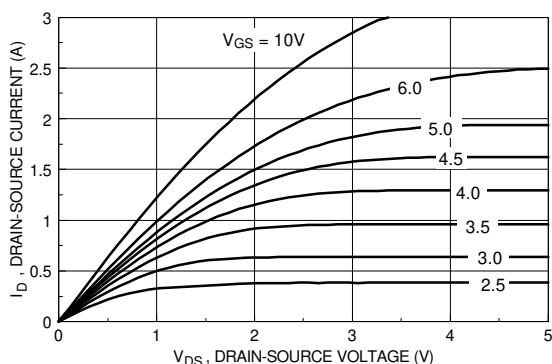


Figure 1. On-Region Characteristics.

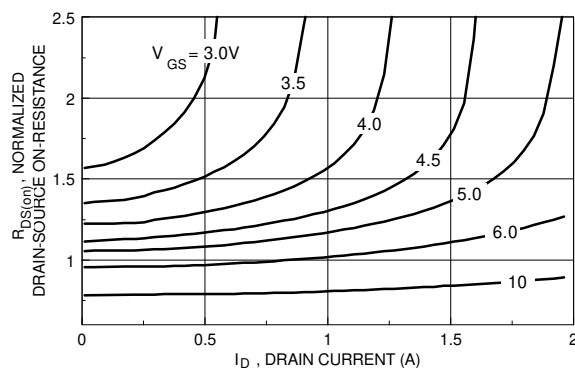


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

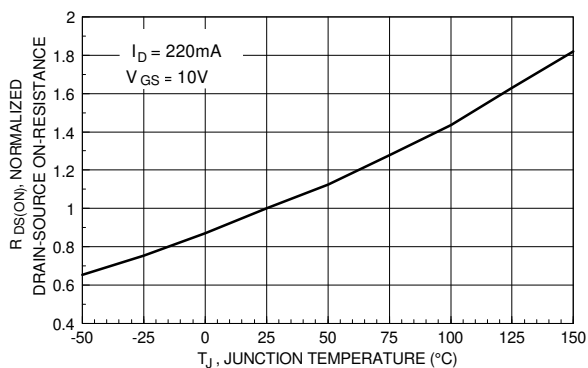


Figure 3. On-Resistance Variation with Temperature.

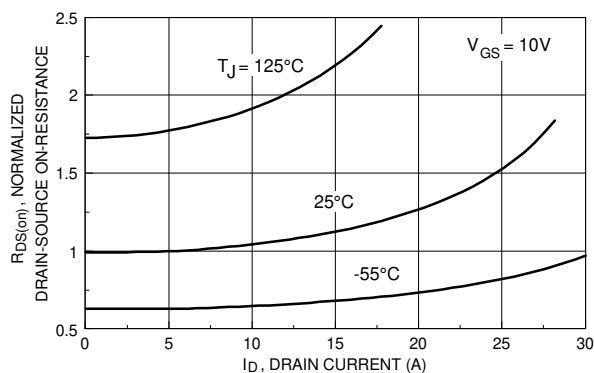


Figure 4. On-Resistance Variation with Drain Current and Temperature.

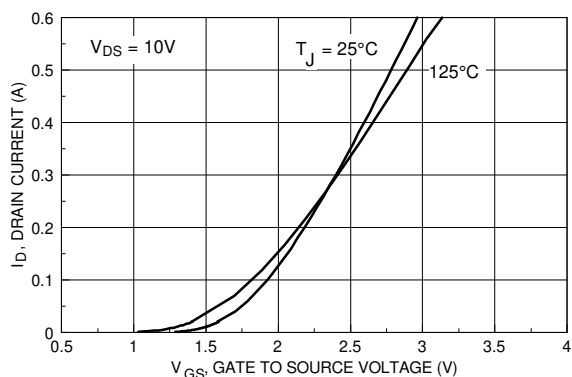


Figure 5. Transfer Characteristics.

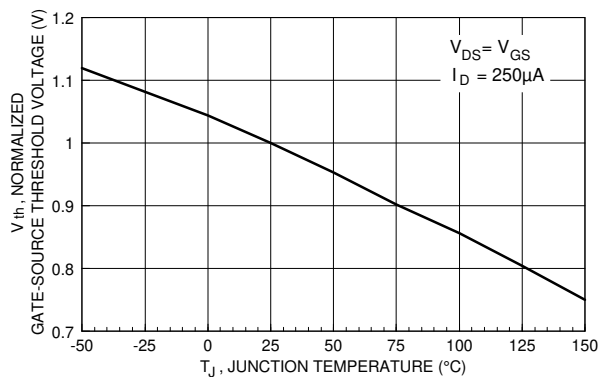


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

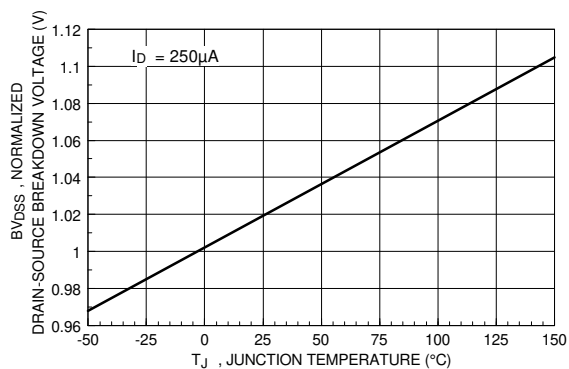


Figure 7. Breakdown Voltage Variation with Temperature.

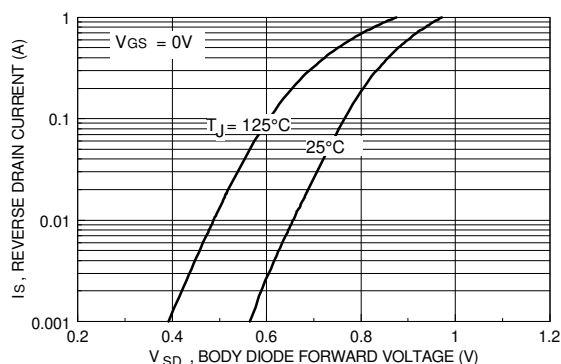


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

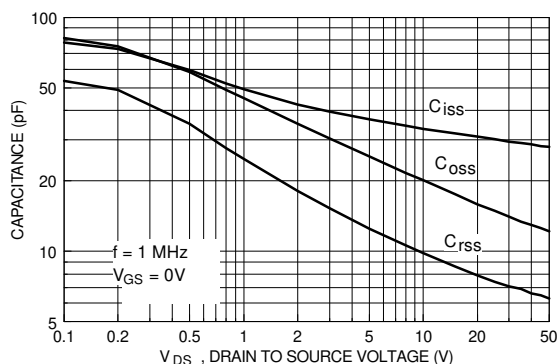


Figure 9. Capacitance Characteristics.

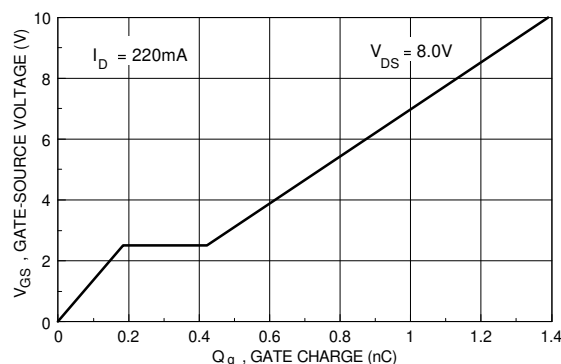


Figure 10. Gate Charge Characteristics.

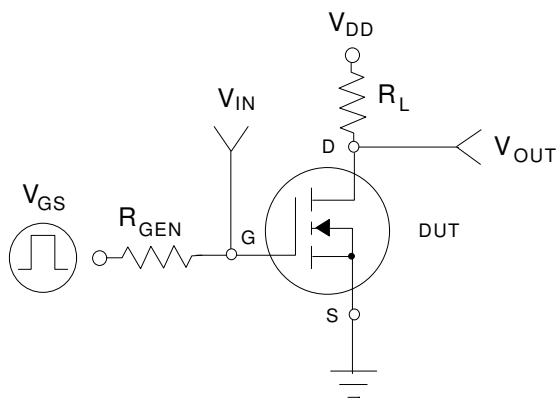


Figure 11. Switching Test Circuit

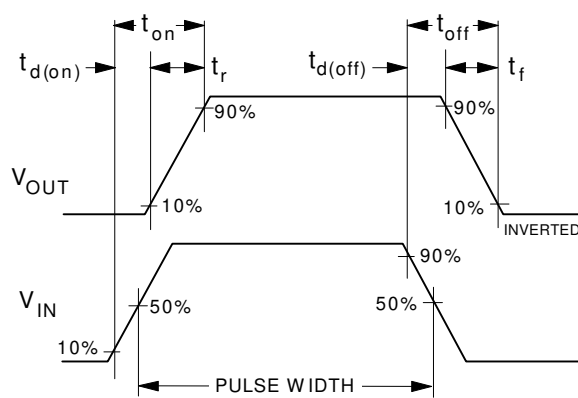


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

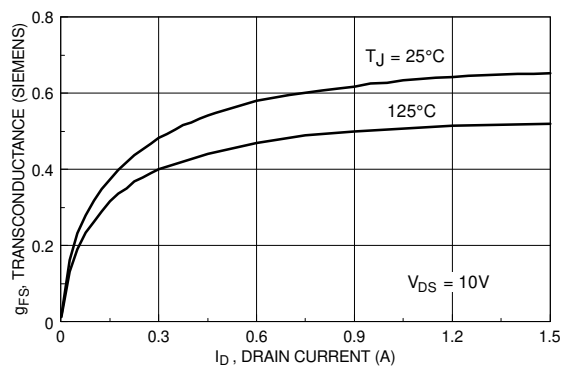


Figure 13. Transconductance Variation with Drain Current and Temperature.

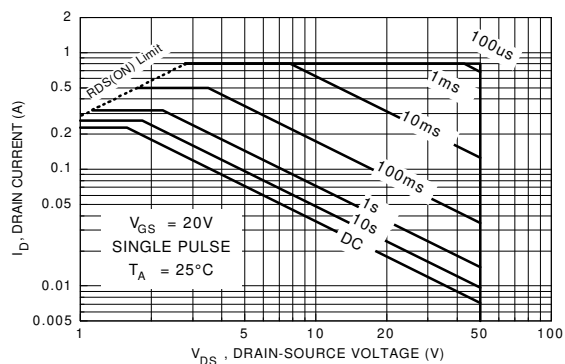


Figure 14. Maximum Safe Operating Area

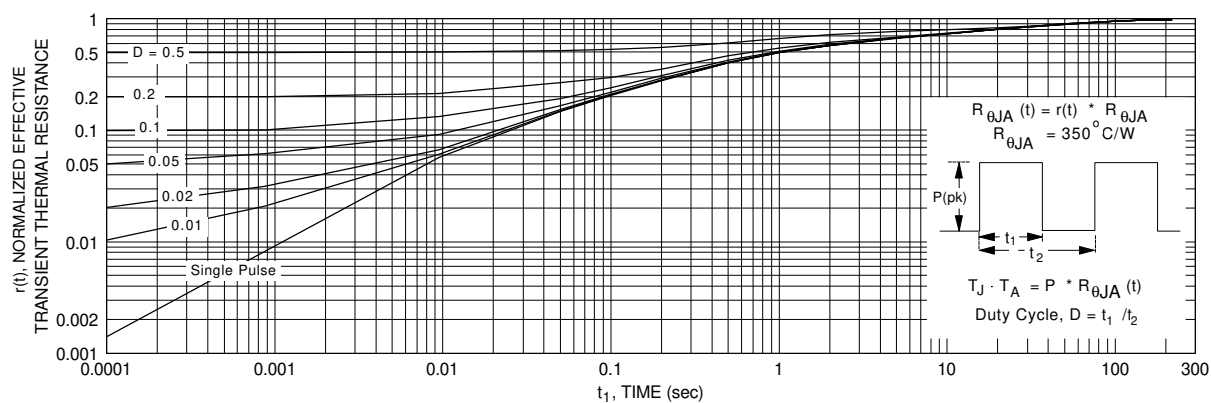


Figure 15. Transient Thermal Response Curve