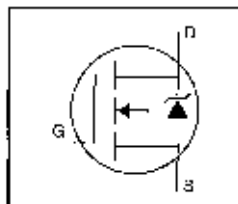


HEXFET® Power MOSFET

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DS} = 500V$$

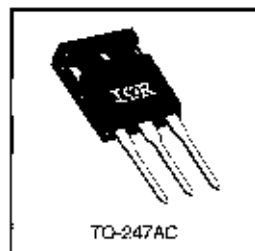
$$R_{DS(on)} = 0.27\Omega$$

$$I_D = 20A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.



DATA
SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} \geq 10V$	20	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} \geq 10V$	13	A
I_{DM}	Pulsed Drain Current	80	A
P_D @ $T_C = 25^\circ C$	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	-20	V
E_{AS}	Single Pulse Avalanche Energy	960	mJ
I_{AS}	Avalanche Current	20	A
E_{AR}	Repetitive Avalanche Energy	28	mJ
dV/dt	Peak Diode Recovery dV/dt	3.5	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to +150	°C
T_{SOL}	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	°C
	Mounting Torque, 6-32 or M3 screw	10 lb-in (1.1 N-m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R_{JC}	Junction-to-Case	—	—	0.45	°C/W
R_{JA}	Case-to-Sink, Flat, Greased Surface	—	0.24	—	°C/W
R_{SA}	Junction-to-Ambient	—	—	40	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{BRDSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$
$\Delta V_{BRDSS}/\Delta T$	Breakdown Voltage Temp. Coefficient	—	0.63	—	$\text{V}/^\circ\text{C}$	Reference to 25°C , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.27	—	Ω	$V_{GS}=10\text{V}$, $I_D=12\text{A}$ (4)
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	—	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
g_{fs}	Forward Transconductance	13	—	—	S	$V_{DS}=50\text{V}$, $I_D=12\text{A}$ (3)
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{GS}=00\text{V}$, $V_{DS}=0\text{V}$
		—	—	250	μA	$V_{GS}=100\text{V}$, $V_{DS}=0\text{V}$, $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{DS}=20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS}=-20\text{V}$
Q_g	Total Gate Charge	—	210	—	nC	$I_D=20\text{A}$
Q_{GS}	Gate-to-Source Charge	—	—	29	nC	$V_{DS}=400\text{V}$
Q_{GD}	Gate-to-Drain ("Miller") Charge	—	—	110	nC	$V_{DS}=10\text{V}$ See Fig. 6 and 13 (4)
t_{don}	Turn-On Delay Time	—	18	—	ns	$V_{DD}=250\text{V}$
t_r	Rise Time	—	59	—	ns	$I_D=20\text{A}$
$t_{f(off)}$	Turn-Off Delay Time	—	110	—	ns	$I_D=4.3\text{A}$
t_f	Fall Time	—	58	—	ns	$I_D=130\text{A}$ See Figure 10 (4)
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 0 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	10	—	nH	
C_{iss}	Input Capacitance	—	4200	—	pF	$V_{GS}=0\text{V}$
C_{oss}	Output Capacitance	—	870	—	pF	$V_{DS}=25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	350	—	pF	$f=1.0\text{MHz}$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_C	Continuous Source Current (Body Diode)	—	—	20	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{RM}	Pulsed Source Current (Body Diode) (4)	—	—	100	A	
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}$, $I_S=20\text{A}$, $V_{GS}=0\text{V}$ (4)
t_r	Reverse Recovery Time	—	570	860	ns	$T_J=25^\circ\text{C}$, $I_F=20\text{A}$
Q_r	Reverse Recovery Charge	—	5.7	8.6	μC	$di/dt=100\text{A}/\mu\text{s}$ (3)
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S , L_D)				

Notes:

- (1) Repetitive rating; pulse width limited by max. junction temperature (See Figure 11); $I_{DSS}=20\text{A}$, $di/dt \leq 160\text{A}/\mu\text{s}$, $V_{DD}=0\text{V}$, $R_{\theta JA} \leq 50^\circ\text{C/W}$, $T_J \leq 150^\circ\text{C}$
- (2) $V_{DD}=50\text{V}$, starting $T_J=25^\circ\text{C}$, $L=4.3\text{nH}$, $R_G=25\Omega$, $I_{AS}=20\text{A}$ (See Figure 12)
- (3) Pulse width $\leq 500\mu\text{s}$; duty cycle $\leq 2\%$.
- (4) $I_{DSS}=20\text{A}$, $di/dt \leq 160\text{A}/\mu\text{s}$, $V_{DD}=0\text{V}$, $R_{\theta JA} \leq 50^\circ\text{C/W}$, $T_J \leq 150^\circ\text{C}$

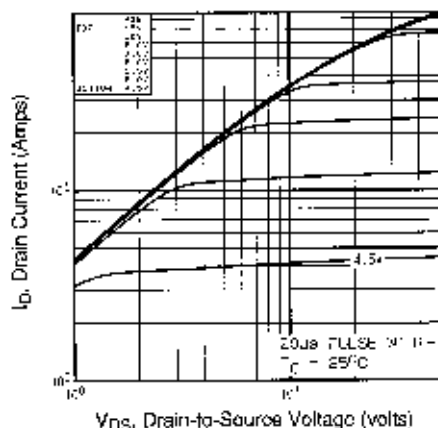


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

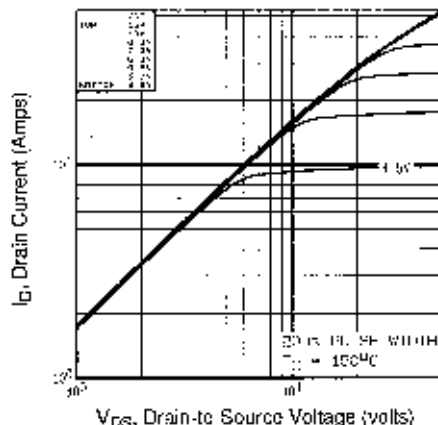


Fig 2. Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$

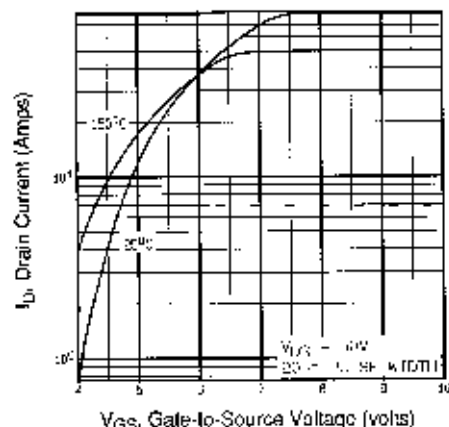


Fig 3. Typical Transfer Characteristics

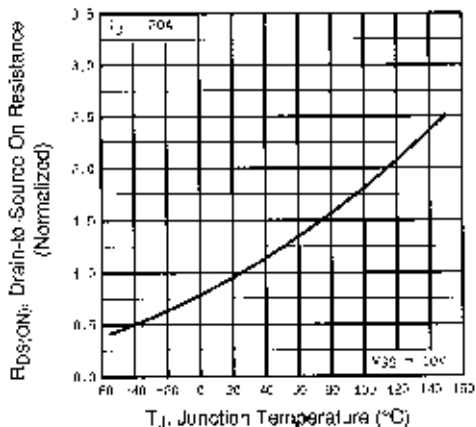


Fig 4. Normalized On-Resistance
Vs. Temperature

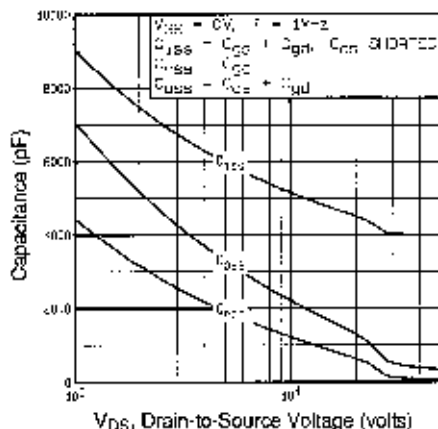


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

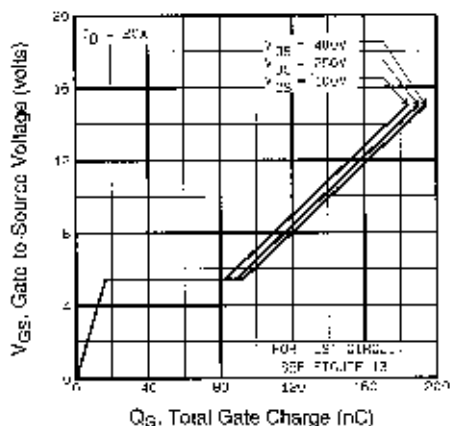


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

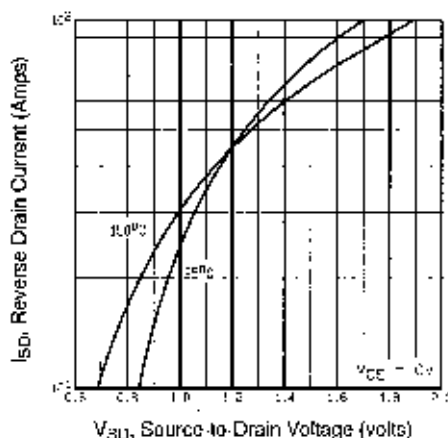


Fig 7. Typical Source-Drain Diode Forward Voltage

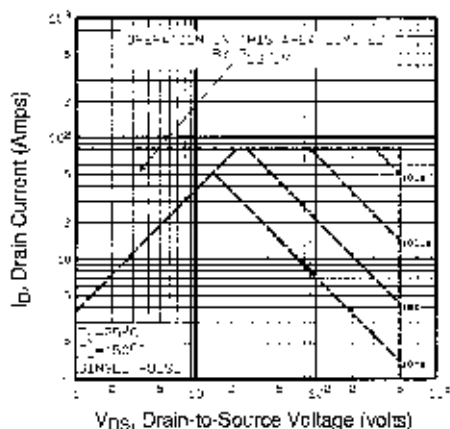


Fig 8. Maximum Safe Operating Area

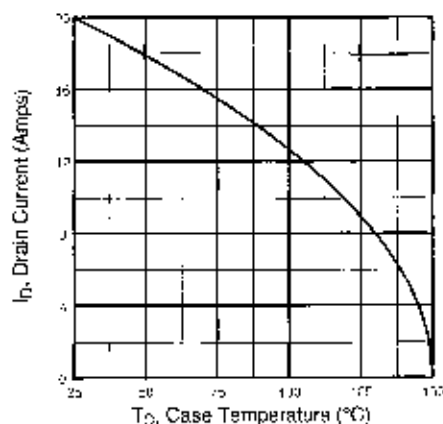


Fig 9. Maximum Drain Current Vs. Case Temperature

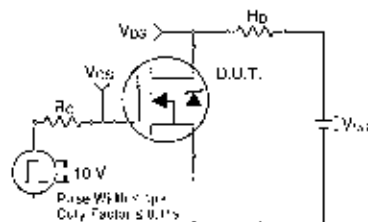


Fig 10a. Switching Time Test Circuit

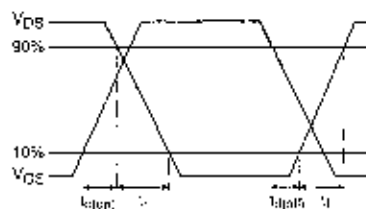


Fig 10b. Switching Time Waveforms

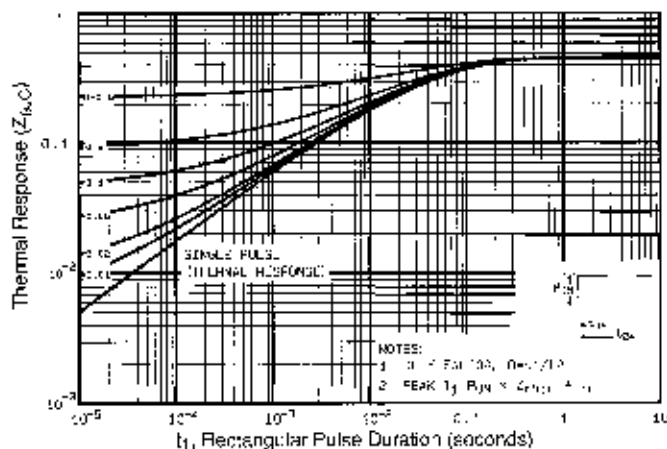


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

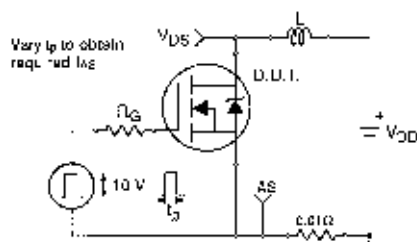


Fig 12a. Unclamped Inductive Test Circuit

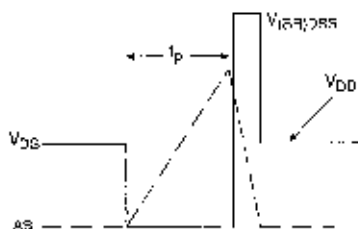


Fig 12b. Unclamped Inductive Waveforms

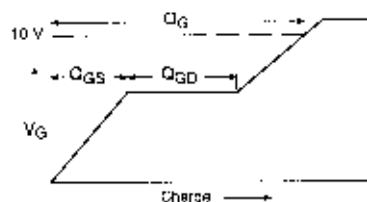


Fig 13a. Basic Gate Charge Waveform

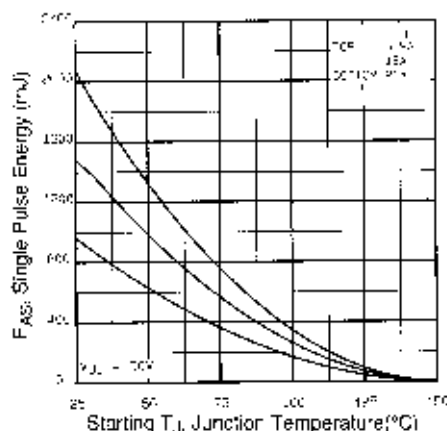


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

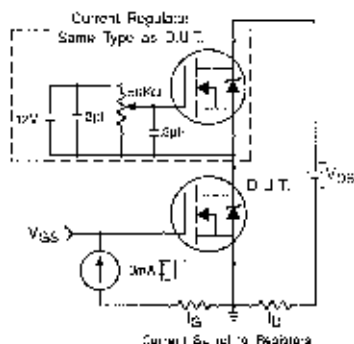


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1511

Appendix C: Part Marking Information – See page 1517

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