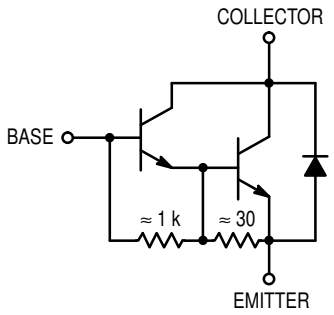
MJ10012
MJH10012

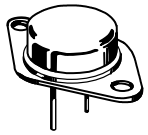
NPN Silicon Power Darlington Transistor

10 AMPERE
POWER TRANSISTORS
DARLINGTON NPN
SILICON
400 VOLTS
175 AND 118 WATTS

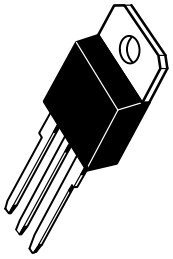
The MJ10012 and MJH10012 are high–voltage, high–current Darlington transistors designed for automotive ignition, switching regulator and motor control applications.

- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 400 Vdc (Min)
- 175 Watts Capability at 50 Volts
- Automotive Functional Tests





CASE 1–07
TO–204AA
(TO–3)
MJ10012



CASE 340D–01
TO–218 TYPE
MJH10012

MAXIMUM RATINGS

Rating	Symbol	MJ10012	MJH10012	Unit
Collector–Emitter Voltage	V_{CEO}	400		Vdc
Collector–Emitter Voltage (R_{BE} = 27 Ω)	V_{CER}	550		Vdc
Collector–Base Voltage	V_{CBO}	600		Vdc
Emitter–Base Voltage	V_{EBO}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C	10 15		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	 175 100 1.0	 118 47.5 1.05	 Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	−55 to +150	°C

THERMAL CHARACTERISTICS

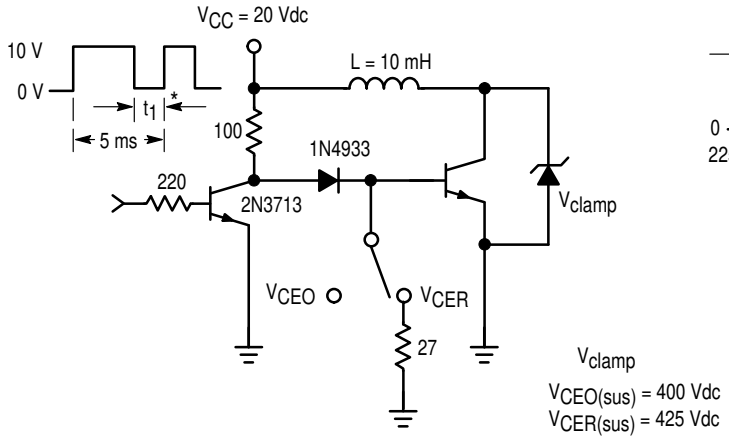
Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.95	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400	—	—	Vdc
Collector–Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, R_{BE} = 27 Ohms, V_{clamp} = Rated V_{CER})	$V_{CER(sus)}$	425	—	—	Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 27 Ohms)	I_{CER}	—	—	1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	40	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 6 0 Vdc) (I_C = 6.0 Adc, V_{CE} = 6.0 Vdc) (I_C = 10 Adc, V_{CE} = 6.0 Vdc)	h_{FE}	 300 100 20	 550 350 150	 — 2000 —	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	 — — —	 — — —	 1 5 2.0 2.5	Vdc
Base Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	 — —	 — —	 2.5 3.0	Vdc
Base Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6.0 Vdc)	$V_{BE(on)}$	—	—	2.8	Vdc
Diode Forward Voltage (I_F = 10 Adc)	V_f	—	2.0	3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	165	350	pF
SWITCHING CHARACTERISTICS					
Storage Time	(V_{CC} = 12 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.3 Adc) Figure 2	t_s	—	7 5	15	µs
Fall Time		t_f	—	5.2	15	µs
FUNCTIONAL TESTS					
Second Breakdown Collector Current with Base–Forward Biased	$I_{S/B}$	See Figure 10			—
Pulsed Energy Test (See Figure 12)	$I_C2L/2$	—	—	180	mJ

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.



* Adjust t_1 such that I_C reaches 200 mA at V_{CE} = V_{clamp}

Figure 1. Sustaining Voltage Test Circuit

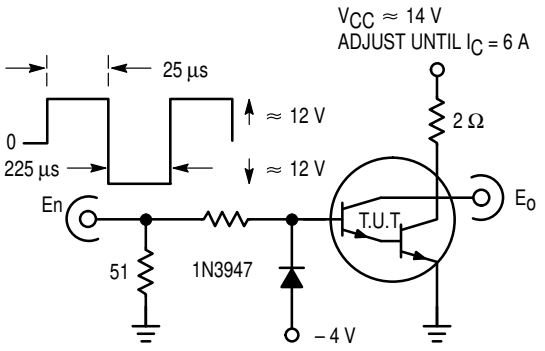


Figure 2. Switching Times Test Circuit

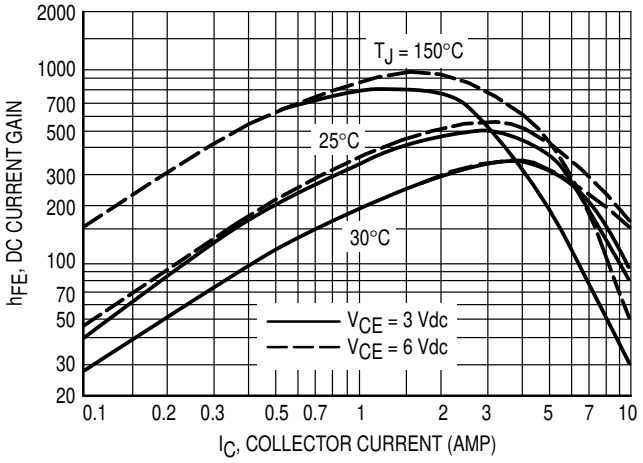


Figure 3. DC Current Gain

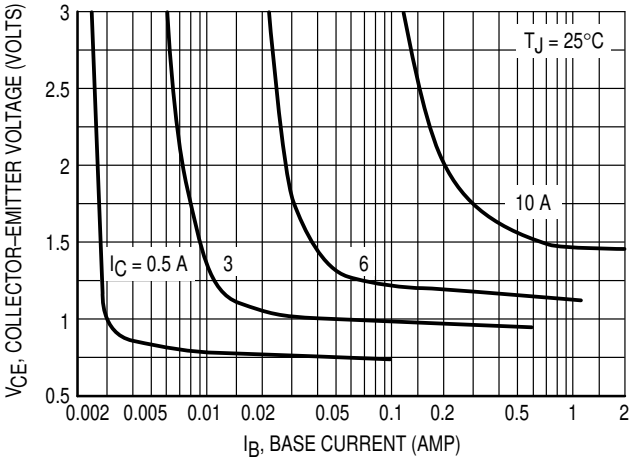


Figure 4. Collector Saturation Region

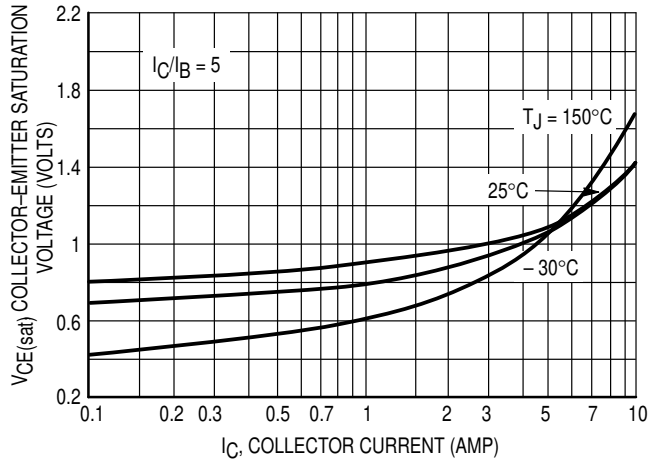


Figure 5. Collector–Emitter Saturation Voltage

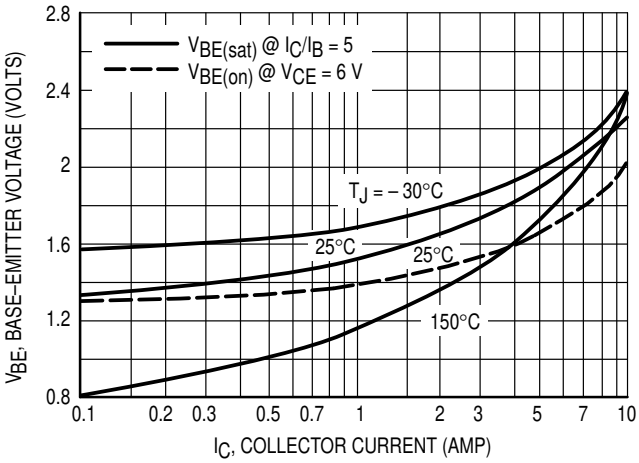


Figure 6. Base–Emitter Voltage

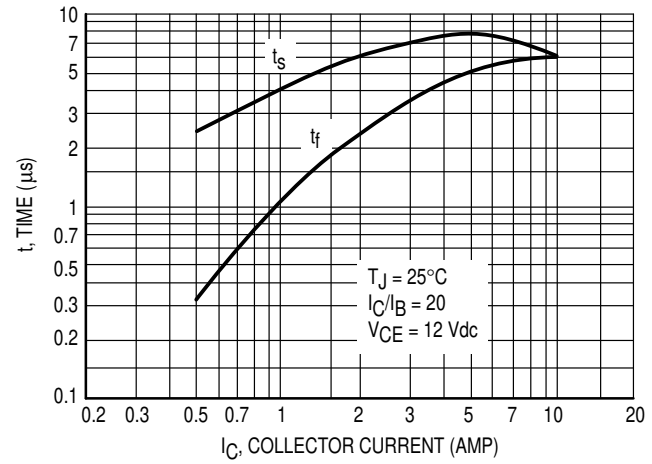


Figure 7. Turn–Off Switching Time

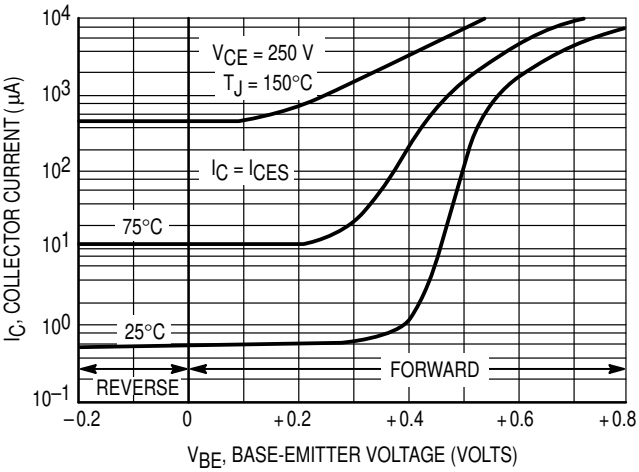


Figure 8. Collector Cutoff Region

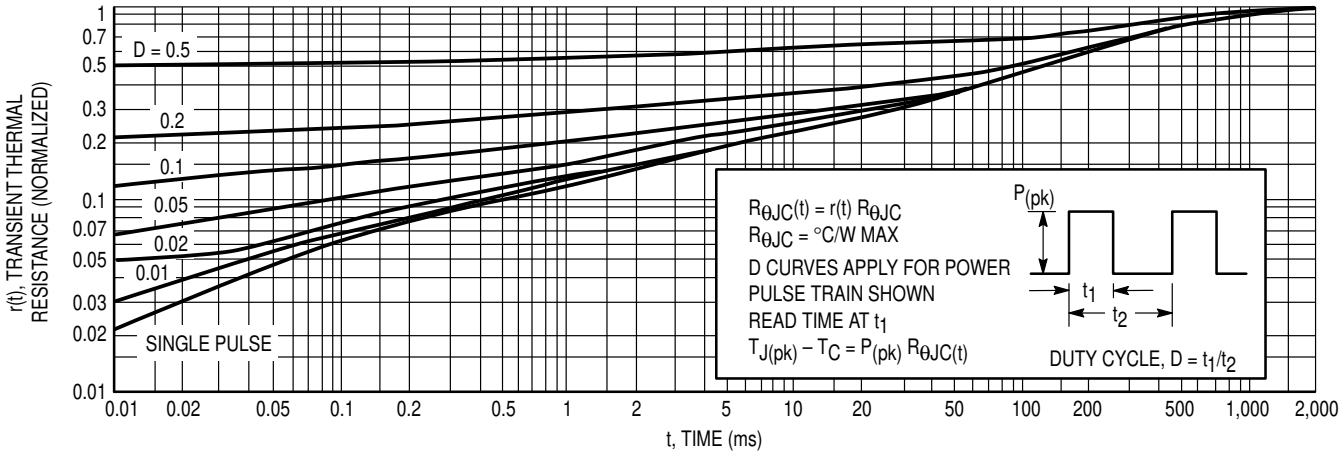


Figure 9. Thermal Response

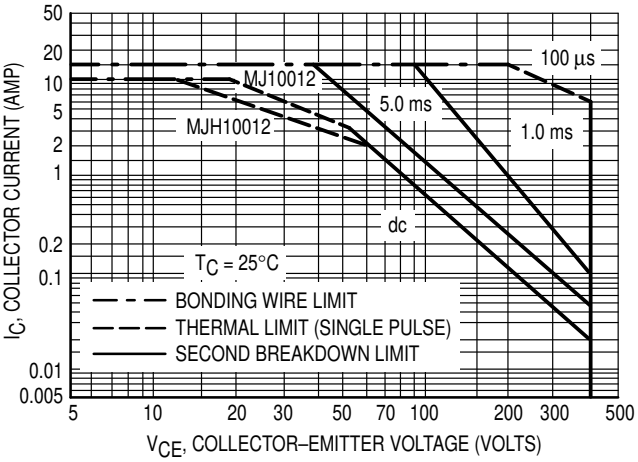


Figure 10. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

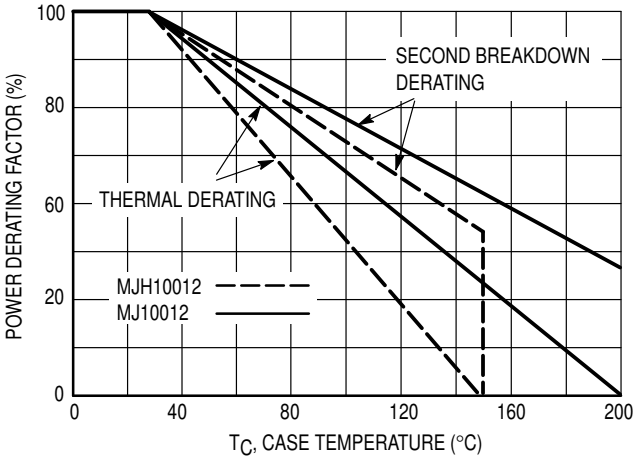
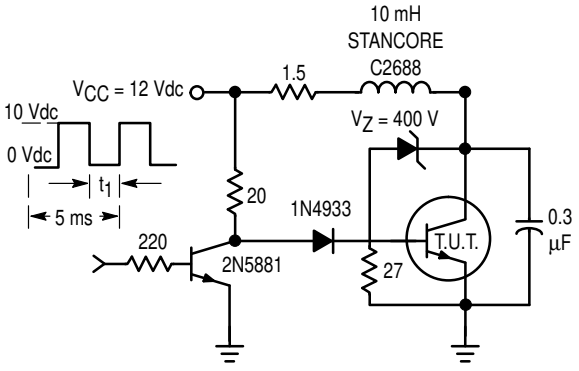


Figure 11. Power Derating

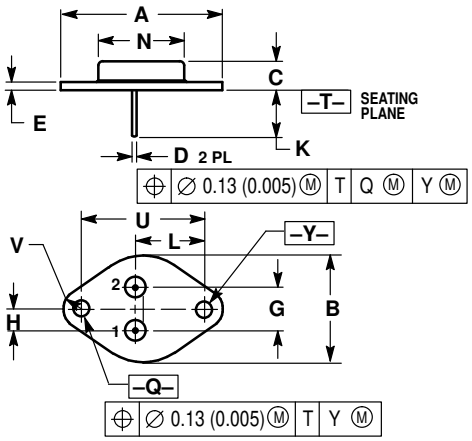


t_1 to be selected such that I_C reaches 6 Adc before switch-off.

NOTE: "Usage Test," Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

Figure 12. Usage Test Circuit

PACKAGE DIMENSIONS

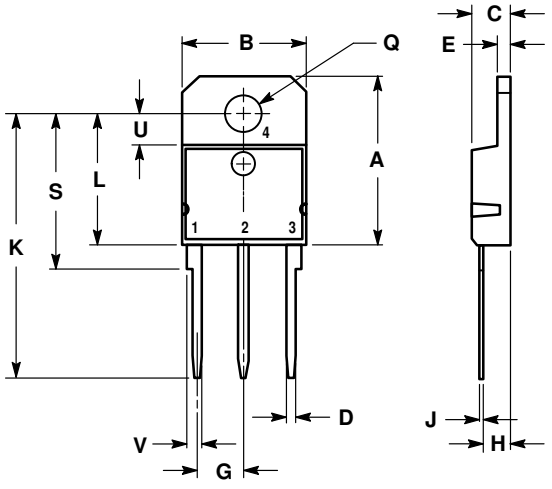


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.00	19.60	0.749	0.771
B	14.00	14.50	0.551	0.570
C	4.20	4.70	0.165	0.185
D	1.00	1.30	0.040	0.051
E	1.45	1.65	0.058	0.064
G	5.21	5.72	0.206	0.225
H	2.60	3.00	0.103	0.118
J	0.40	0.60	0.016	0.023
K	28.50	32.00	1.123	1.259
L	14.70	15.30	0.579	0.602
Q	4.00	4.25	0.158	0.167
S	17.50	18.10	0.689	0.712
U	3.40	3.80	0.134	0.149
V	1.50	2.00	0.060	0.078

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340D–01
SOT 93, TO–218 TYPE
ISSUE A

How to reach us:
USA / **EUROPE**: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298