Complementary Plastic Silicon Power Transistors

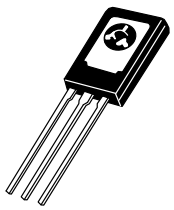
. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc — MJE171, MJE181
  = 80 Vdc — MJE172, MJE182
- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 0.5 Adc
  = 12 (Min) @ I_C = 1.5 Adc
- Current–Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages —
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}

PNP
MJE171*
MJE172*
NPN
MJE181*
MJE182*

*Motorola Preferred Device

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–80 VOLTS
12.5 WATTS



CASE 77–08
TO–225AA

MAXIMUM RATINGS

Rating	Symbol	MJE171 MJE181	MJE172 MJE182	Unit
Collector–Base Voltage	V_{CB}	80	100	Vdc
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	3.0 6.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012		Watts W/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

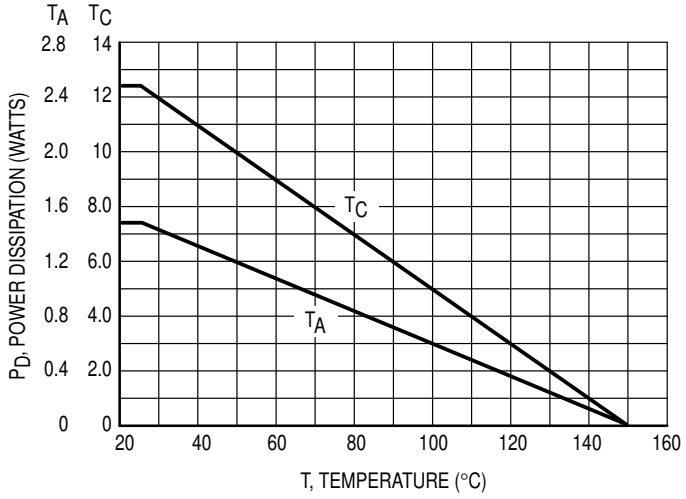


Figure 1. Power Derating

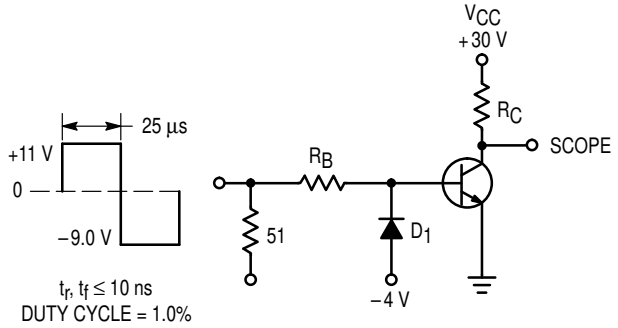
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	MJE171, MJE181	$V_{CEO(sus)}$	60	—	Vdc
	MJE172, MJE182		80	—	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	MJE171, MJE181		—	0.1	
(V_{CB} = 100 Vdc, I_E = 0)	MJE172, MJE182		—	0.1	
(V_{CB} = 80 Vdc, I_E = 0, T_C = 150°C)	MJE171, MJE181		—	0.1	mAdc
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	MJE172, MJE182		—	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	250	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	—	
(I_C = 1.5 Adc, V_{CE} = 1.0 Vdc)			12	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			—	0.3	
(I_C = 1.5 Adc, I_B = 150 mAdc)			—	0.9	
(I_C = 3.0 Adc, I_B = 600 mAdc)			—	1.7	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			—	1.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			—	2.0	
Base–Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	50	—	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE171/MJE172		—	60	
	MJE181/MJE182		—	40	

(1) $f_T = |h_{fe}| \bullet f_{test}$.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

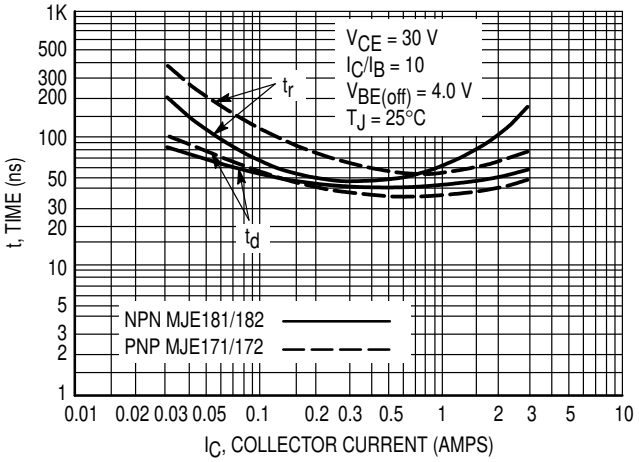


Figure 3. Turn–On Time

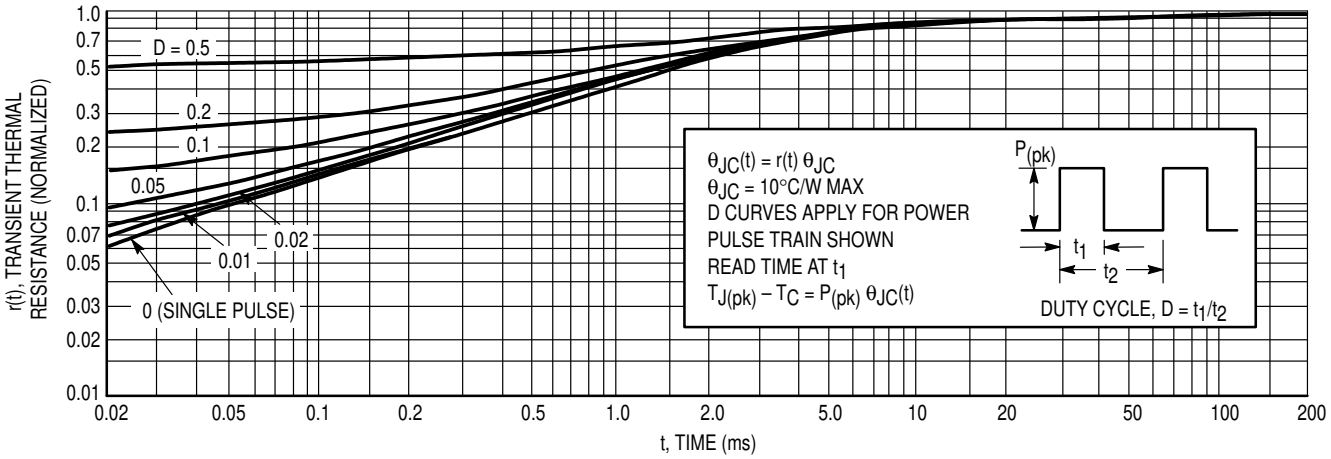


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

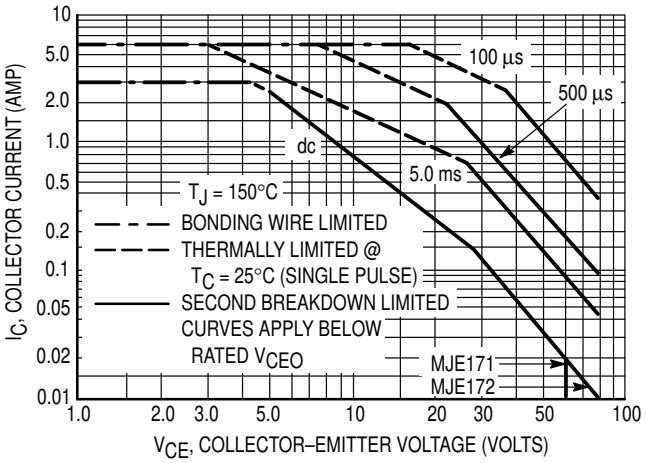


Figure 5. MJE171, MJE172

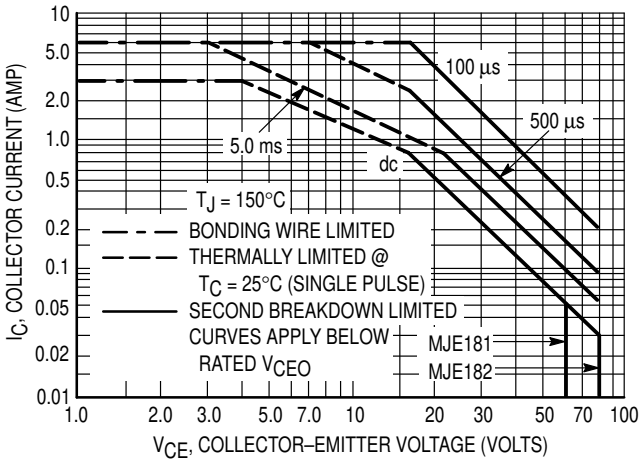


Figure 6. MJE181, MJE182

There are two limitations on the power handling ability of a transistor — average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

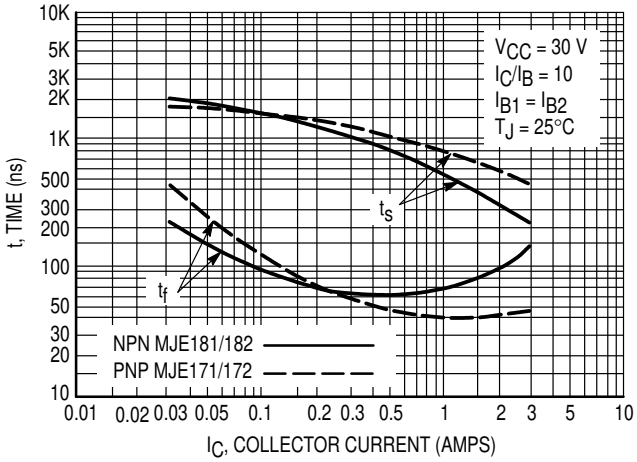


Figure 7. Turn–Off Time

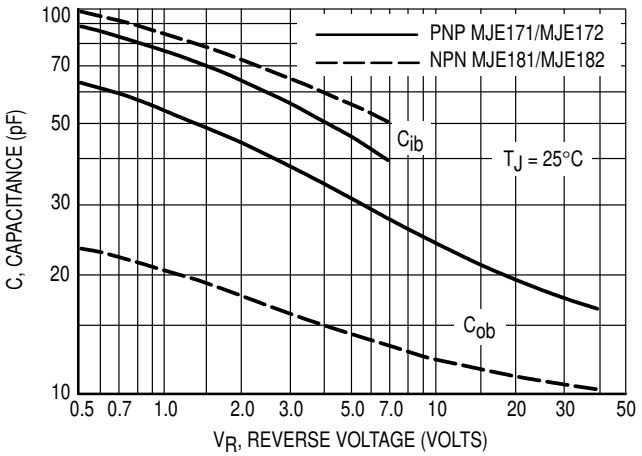
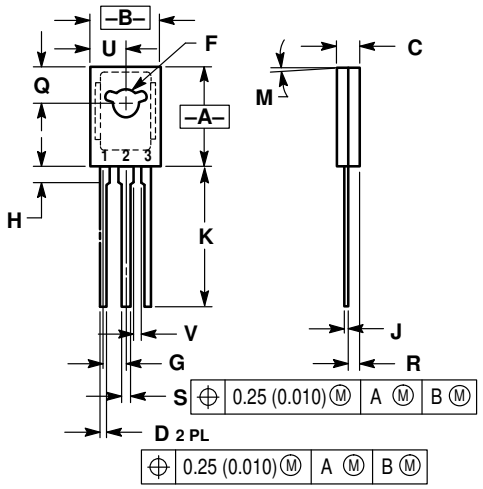


Figure 8. Capacitance

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.055	1.15	1.39
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	—	1.02	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

CASE 77–08
TO–225AA
ISSUE V

How to reach us:
USA / **EUROPE**: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298