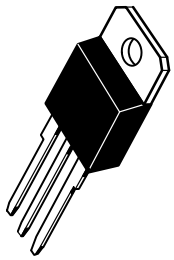
NPN
MJE4342
MJE4343
PNP
MJE4352
MJE4353

High-Voltage — High Power Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector–Emitter Sustaining Voltage —
  NPN PNP
  $V_{CEO(sus)}$ = 140 Vdc — MJE4342 MJE4352
  = 160 Vdc — MJE4343 MJE4353
- High DC Current Gain — @ I_C = 8.0 Adc
  h_{FE} = 35 (Typ)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 8.0 Adc

16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140–160 VOLTS



CASE 340D–01
TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	MJE4342 MJE4352	MJE4343 MJE4353	Unit
Collector–Emitter Voltage	V_{CEO}	140	160	Vdc
Collector–Base Voltage	V_{CB}	140	160	Vdc
Emitter–Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak (1)	I_C	16 20		Adc
Base Current — Continuous	I_B	5.0		Adc
Total Power Dissipation @ T_C = 25°C	P_D	125		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

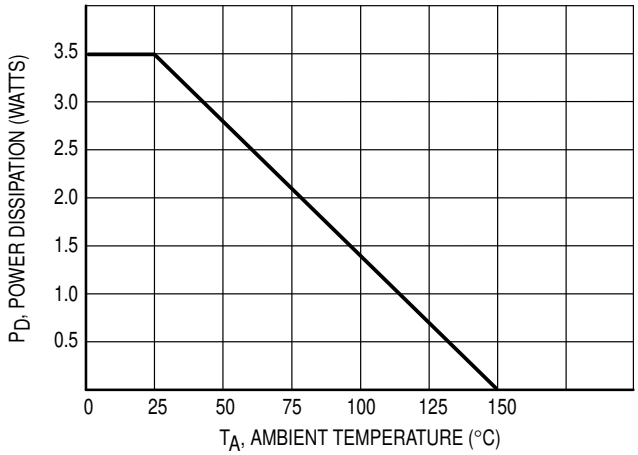


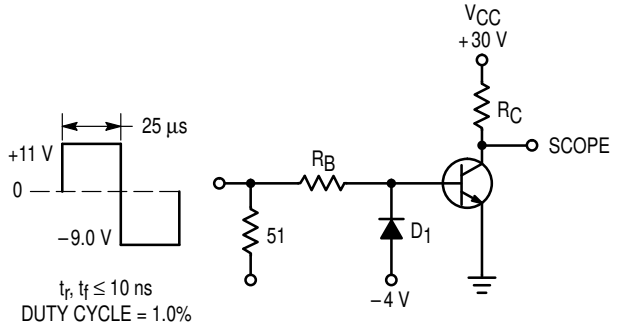
Figure 1. Power Derating
Reference: Ambient Temperature

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	MJE4342, MJE4352 MJE4343, MJE4353	$V_{CEO(sus)}$	140 160	— —	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 70 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0	 MJE4342, MJE4352 MJE4343, MJE4353	I_{CEO}	— —	750 750	μAdc
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	— —	1.0 5.0	mAdc
Collector–Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	750	μAdc
Emitter–Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 15 8.0	 35 (Typ) 15 (Typ)	—
Collector–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 800 mA) (I_C = 16 Adc, I_B = 2.0 Adc)		$V_{CE(sat)}$	 — —	 2.0 3.5	Vdc
Base–Emitter Saturation Voltage (I_C = 16 Adc, I_B = 2.0 Adc)		$V_{BE(sat)}$	—	3.9	Vdc
Base–Emitter On Voltage (I_C = 16 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	3.9	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	800	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

Note: Reverse polarities to test PNP devices.

Figure 2. Switching Times Test Circuit

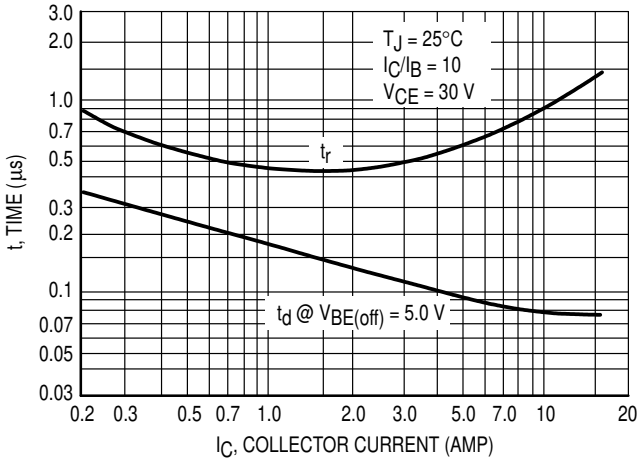


Figure 3. Typical Turn–On Time

TYPICAL CHARACTERISTICS

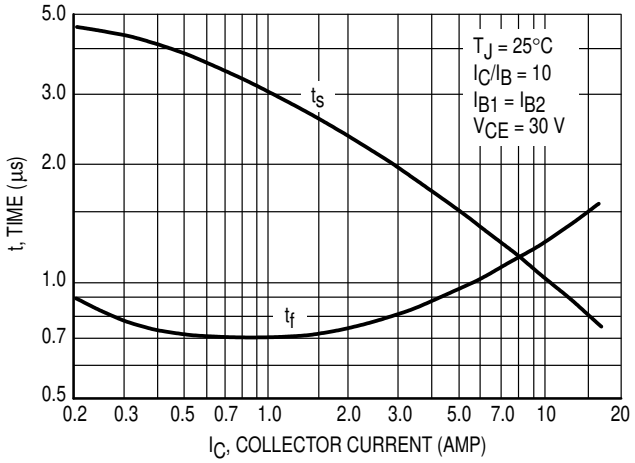


Figure 4. Turn–Off Time

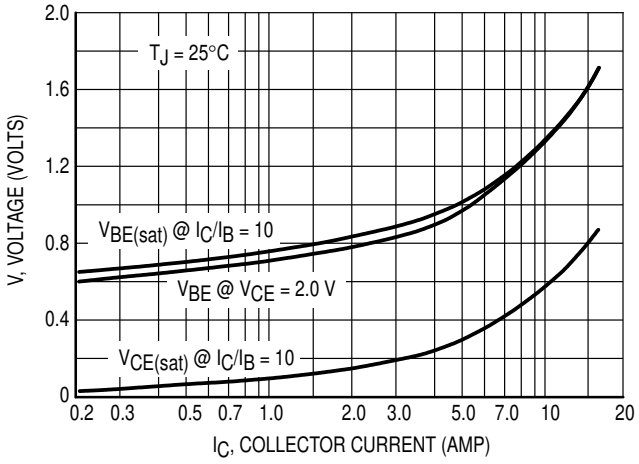


Figure 5. On Voltages

DC CURRENT GAIN

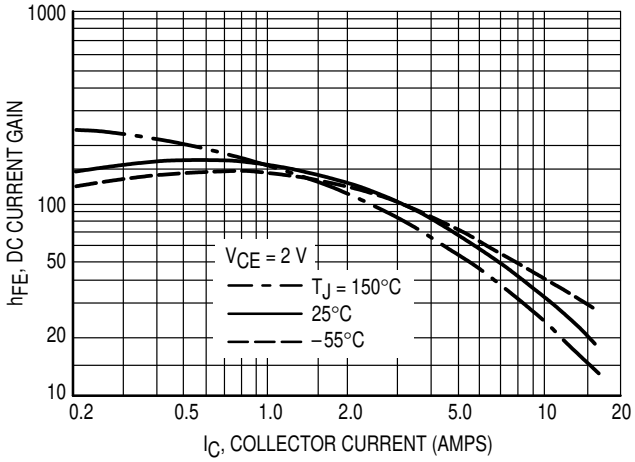


Figure 6. MJE4340 Series (NPN)

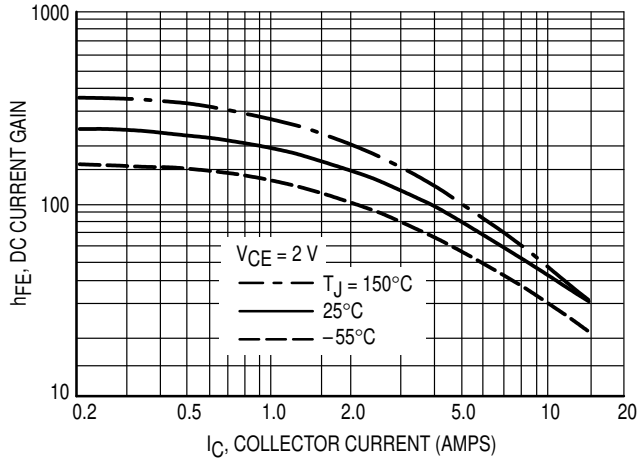


Figure 7. MJE4350 Series (PNP)

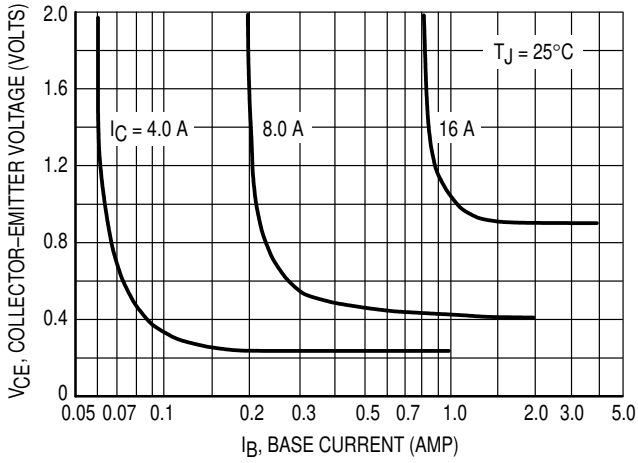


Figure 8. Collector Saturation Region

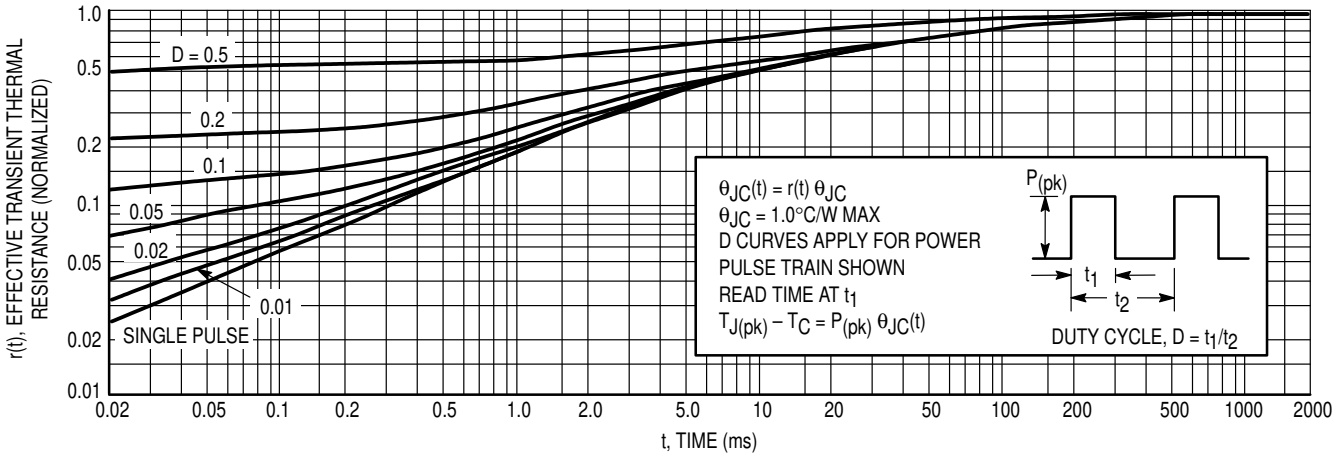


Figure 9. Thermal Response

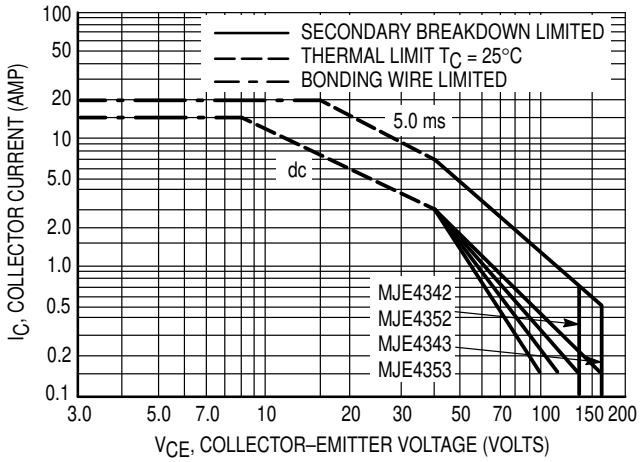


Figure 10. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

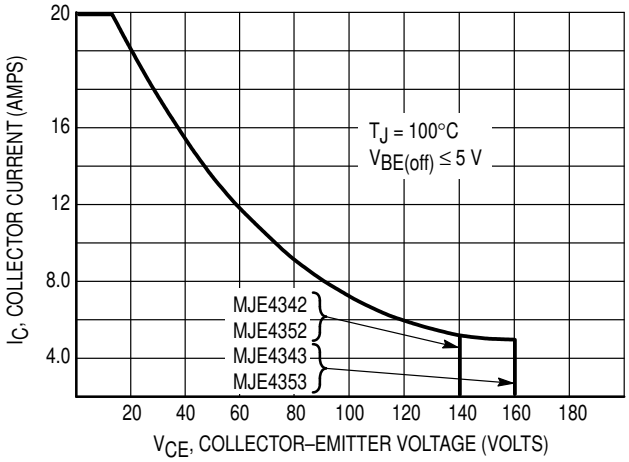
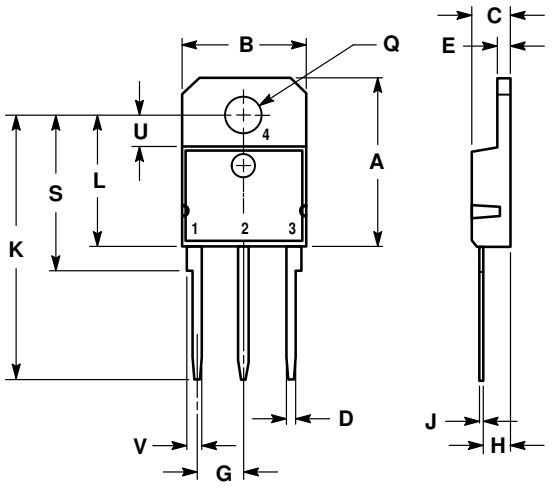


Figure 11. Maximum Reverse Bias Safe Operating Area

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.00	19.60	0.749	0.771
B	14.00	14.50	0.551	0.570
C	4.20	4.70	0.165	0.185
D	1.00	1.30	0.040	0.051
E	1.45	1.65	0.058	0.064
G	5.21	5.72	0.206	0.225
H	2.60	3.00	0.103	0.118
J	0.40	0.60	0.016	0.023
K	28.50	32.00	1.123	1.259
L	14.70	15.30	0.579	0.602
Q	4.00	4.25	0.158	0.167
S	17.50	18.10	0.689	0.712
U	3.40	3.80	0.134	0.149
V	1.50	2.00	0.060	0.078

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340D–01
TO–218 TYPE
ISSUE A

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